CLAIMS

What is claimed is:

1. An apparatus comprising:

a configurable link which permits

a first level of access if a computer's central processing unit (CPU) is in a first power management state; and

a second level of access if the computer's CPU is in a second power management state.

2. The device of claim 1, wherein the first power management state and the second power management state each comprises a set of power management states.

3. The apparatus of claim 1, further comprising:

a first peripheral device communicatively coupled to the configurable link wherein the first level of access the peripheral device is capable of operating as a conventional peripheral device.

4. The apparatus of claim 1, further comprising:

a first peripheral device communicatively coupled to the configurable link wherein the second level of access the peripheral device is capable of operating as the default bus master for the computer without assistance from the CPU.

5. The apparatus of claim 4, wherein a peripheral device coupled to the configurable link causes the configurable link to operate in the second level of access when the CPU is in a second power management state

6. The apparatus of claim 1, wherein the second power management state the computer's CPU is in a sleeping state.

7. The apparatus of claim 1, wherein the second power management state includes power modes S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

8. The apparatus of claim 1, wherein the second level of access the transfer rate over the configurable link is different than in the first level of access.

9. The apparatus of claim 1, further comprising:

a first peripheral device coupled to the configurable link; and

an input/output hub communicatively coupling the configurable link and the central processing unit (CPU).

10. The apparatus of claim 9, wherein the first level of access, the CPU manages the input/output hub to control communications to and from the first peripheral device.

11. The apparatus of claim 9, wherein the second level of access, the configurable link enables the first peripheral device to manage the

input/output hub to control communications to and from the first peripheral device.

12. The apparatus of claim 9, further comprising

a second peripheral device communicatively coupled to the input/output hub.

13. The apparatus of claim 12, wherein the second level of access, the first peripheral device can communicate directly with the second peripheral device without assistance from the CPU.

14. A method comprising:

configuring a link to provide a first level of access to a computer's resources if the computer's central processing unit (CPU) is in a first power management state; and

configuring the link to provide a second level of access to the computer's resources if the computer's CPU is in a second power management state.

15. The method of claim 14, further comprising:

coupling a peripheral device to the configurable link wherein the second level of access the peripheral device is capable of operating as the default bus master for the computer.

16. The method of claim 15, wherein the first level of access the peripheral is capable of operating as a conventional peripheral device.

17. The method of claim 14, wherein the second power management state the computer's CPU is in a sleeping state.

18. The method of claim 14, wherein the second power management state includes power modes S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

19. The method of claim 14, wherein a peripheral device coupled to the configurable link causes the configurable link to operate in the second level of access when the CPU is in a second power management state.

20. The method of claim 14, wherein configuring the link to provide a second level of access also requires configuring an input/output hub to which the link couples to allow the peripheral device to become the default bus master.

21. A system, comprising:

a sub-system to detect the power management state of a central processor;

a sub-system to determine whether the central processor is in a first power management state or a second power management state;

a sub-system to allow the central processor to manage data flow over an input/output hub if the central processor is in a first power management state; and

a sub-system to configure a link coupling the input/output hub to a first peripheral device to allow the first peripheral device to manage data flow over the hub if the central processor is in a second power management state.

22. The system of claim 21, further comprising:

a sub-system to initiate a data transfer from the first peripheral device if the central processor is in the second power management state.

23. The system of claim 21, further comprising:

a sub-system to buffer data at the first peripheral device if the central processor is in the second power management state.

24. The system of claim 21, further comprising:

a sub-system to allow the first peripheral device to directly access and communicate with a second peripheral device without assistance from the central processor.

25. The system of claim 21, further comprising:

a sub-system to delay the central processor from transitioning from the second power management state to the first power management state.